IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES
(Attorney Docket No. 13757US03)

In The Application Of:

Amir Morad, *et al.*

Electronically Filed on May 16, 2011

Serial No.: 10/776,541

Filed: February 10, 2004

For: SYSTEM AND METHOD
FOR VIDEO AND AUDIO
ENCODING ON A SINGLE CHIP

Examiner: VO, TUNG T.

Group Art Unit: 2621

Confirmation No.: 3126

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the final rejection of claims 10-36 of the present application. This Appeal Brief is timely because it is being filed within three months from the date on which the Notice of Appeal was filed and is accompanied by a request for a one month extension of time.

REAL PARTY IN INTEREST
(37 C.F.R. § 41.37(C)(1)(I))

The real party in interest is Broadcom Corporation, a corporation organized under the laws of the state of California, having a place of business at 5300 California Avenue, Irvine, California 92617, which has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 014640, Frame 0732 in the PTO Assignment Search room.

RELATED APPEALS AND INTERFERENCES
(37 C.F.R. § 41.37(C)(1)(II))

Appellants are unaware of any related appeals or interferences.

STATUS OF THE CLAIMS
(37 C.F.R. § 41.37(C)(1)(III))

The present application includes pending claims 10-36 all of which have been rejected. Appellants identify claims 10-36 as the claims that are being appealed. The text of the pending claims is provided in the Claims Appendix.

STATUS OF AMENDMENTS
(37 C.F.R. § 41.37(C)(1)(IV))

No claims were amended following issuance of the Final Office Action on November 16, 2010. No claim amendments are currently pending.

SUMMARY OF CLAIMED SUBJECT MATTER
(37 C.F.R. § 41.37(C)(1)(V))

Independent claim 10 recites the following:

A single-chip audio/video encoder device comprising, on a single integrated circuit: [1]

multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;[2]

a first encoder that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;[3]

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[1] *See, e.g.,* present application at p. 9, lines 10-13; p. 11, lines 10-13; Fig. 5.

[2] *See, e.g.*, present application at Fig. 5, ref. 114; p. 20, ¶ 63, lines 1-9; *see also* Application Serial No. 60/296,766 (incorporated by reference into present application at p. 1, lines 15-18) ("766 Application") at p. 9 ("The two compressed video streams and two compressed audio streams are delivered to a highly programmable multiplexing unit. . . . The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")

[3] *See, e.g.,* present application at Fig. 5, ref. 102, 105, 106, 108, 112, and 113; p. 14, ¶ 43, line 1 to ¶ 45, line 5; p. 16, ¶ 51, line 1 to p. 20, ¶ 62, line 9; *see also* 766 Application

a second encoder that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;[4]

control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;[5]

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device;[6] and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.[7]

Independent claim 24 recites the following:

A single-chip audio/video encoder device comprising, on a single integrated circuit:[8]

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at p. 7, block diagram including VIBx2, MEFx2, P4x2, DSPx2, BSMx2, and AUDXx2; *see also id.* at p. 9 ("Integrated features . . . include two MPEG-2 video encoders [and] two high fidelity audio encoder DSPs . . . .")

[4] *See, e.g.,* present application at Fig. 5, ref. 102, 105, 106, 108, 112, and 113; p. 14, ¶ 43, line 1 to ¶ 45, line 5; p. 16, ¶ 51, line 1 to p. 20, ¶ 62, line 9; *see also* 766 Application at p. 7, block diagram including VIBx2, MEFx2, P4x2, DSPx2, BSMx2, and AUDXx2; *see also id.* at p. 9 ("Integrated features . . . include two MPEG-2 video encoders [and] two high fidelity audio encoder DSPs . . . .")

[5] *See, e.g.,* present application at p. 20, ¶ 64, lines 1-7; Fig. 5, Global Controller 104.

[6] *See, e.g.* 766 Application at p. 9 ("The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")

[7] *See, e.g.* 766 Application at p. 9 ("The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")

[8] *See, e.g.,* present application at p. 9, lines 10-13; p. 11, lines 10-13; Fig. 5.

control circuitry[9] that synchronizes a first encoder,[10] a second encoder,[11] and multiplexing circuitry[12] to produce a first multiplexed stream from first uncompressed video data, first uncompressed audio data, second uncompressed video data, and second uncompressed audio data, when the multiplexing circuitry operates in a first mode, and to concurrently produce the first multiplexed stream from the first uncompressed video data and the first uncompressed audio data and a second multiplexed stream from the second uncompressed video data and the second uncompressed audio data, when the multiplexing circuitry operates in a second operating mode;

a first input for receiving the first uncompressed video data and first uncompressed audio data from a first source external to the device;[13]

a second input for receiving second uncompressed video data and second uncompressed audio data from a second source external to the device;[14]

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[9] *See, e.g.,* present application at p. 20, ¶ 64, lines 1-7; Fig. 5, Global Controller 104.
[10] *See, e.g.,* present application at Fig. 5, ref. 102, 105, 106, 108, 112, and 113; p. 14, ¶ 43, line 1 to ¶ 45, line 5; p. 16, ¶ 51, line 1 to p. 20, ¶ 62, line 9; *see also* 766 Application at p. 7, block diagram including VIBx2, MEFx2, P4x2, DSPx2, BSMx2, and AUDXx2; *see also id.* at p. 9 ("Integrated features . . . include two MPEG-2 video encoders [and] two high fidelity audio encoder DSPs . . . .")
[11] *See, e.g.,* present application at Fig. 5, ref. 102, 105, 106, 108, 112, and 113; p. 14, ¶ 43, line 1 to ¶ 45, line 5; p. 16, ¶ 51, line 1 to p. 20, ¶ 62, line 9; *see also* 766 Application at p. 7, block diagram including VIBx2, MEFx2, P4x2, DSPx2, BSMx2, and AUDXx2; *see also id.* at p. 9 ("Integrated features . . . include two MPEG-2 video encoders [and] two high fidelity audio encoder DSPs . . . .")
[12] *See, e.g.*, present application at Fig. 5, ref. 114; p. 20, ¶ 63, lines 1-9; *See, e.g.*, 766 Application at p. 9 ("The two compressed video streams and two compressed audio streams are delivered to a highly programmable multiplexing unit. . . . The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")
[13] *See, e.g.,* 766 Application at p. 9 ("Integral features . . . include two MPEG-2

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device;[15] and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.[16]

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(C)(1)(VI))

Claims 10-20 and 24-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 5,825,430 ("Adolph") in view of U.S. 6,490,250 ("Hinchley").

Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph and Hinchley, and further in view of U.S. 6,516,031 ("Ishihara").

Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph, Hinchley, and Ishihara, and further in view of U.S. 5,448,310 ("Kopet").

Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. 6,665,872 ("Krishnamurthy") in view of Adolph.

Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy and Adolph, and further in view of US 6,519,289 ("Bruck").

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encoders [and] two audio encoder DSPs.

[14] *See, e.g., See, e.g.,* 766 Application at p. 9 ("Integral features . . . include two MPEG-2 encoders [and] two audio encoder DSPs.

[15] *See, e.g.,* 766 Application at p. 9 ("The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")

[16] *See, e.g.,* 766 Application at p. 9 ("The multiplexer can output two multiplexed streams, each containing one video stream and one audio stream, or one multiplexed stream containing all the four input streams.")

Claims 14, 17-19, 27, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy and Adolph, in further view of Hinchley.

Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy and Adolph, and further in view of U.S. 6,823,013 ("Boice").

Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy and Adolph, and further in view of Kopet.

ARGUMENT
(37 C.F.R. § 41.37(C)(1)(VII))

All of the claims are rejected for alleged reasons of obviousness. The MPEP states the following regarding the requirements for establishing a *prima facie* case of obviousness:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" *See id.*, § 2143.01. Furthermore, in order

to render the claims obvious, the asserted prior art combination must **teach or suggest each and every claim feature**. *See In re Royka*, 490 F.2d 981 (CCPA 1974) (to establish *prima facie* obviousness of a claimed invention, all the claim features must be taught or suggested by the prior art);[17] *see also In re Wada and Murphy*, Appeal 2007-3733, citing *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (A proper obviousness determination requires that an Examiner make "a searching comparison of the claimed invention – **including all its limitations** – with the teaching of the prior art.")

If a *prima facie* case of obviousness is not established, Appellants have no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

With these principles in mind, Appellants now turn to the claim rejections in particular.

I. CLAIMS 10-20 AND 24-33 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF ADOLPH AND HINCHLEY

A. Independent Claims 10 And 24

Claim 10 is patentable because the proposed combination of Adolph and Hinchley fails to disclose or suggest at least a "single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first

[17] Emphasis added except where noted otherwise.

multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio," as required by claim 10. The Examiner alleges this claim limitation is disclosed in Adolph as follows:

> Re claims 10 and 24, Adolph discloses a audio/video encoder device (fig. 3, a single device) comprising, on a single integrated circuit:
>
> multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode),
>
> which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and
>
> which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3);

(6/16/2010 Office Action at p. 2.)[18] Accordingly, the Examiner identifies the entirety of FIG. 3 of Adolph as teaching Appellants' claimed "audio/video encoder device," and the portion of FIG. 3 labeled "EMUX" as teaching Appellants' claimed "multiplexer circuitry." (*Id.*) The Examiner also interprets the "performing of MMUX" of FIG. 3 of Adolph as teaching Appellants' "first mode," and the "performing of MUX 1 and MUX 2" of FIG. 3 of Adolph as teaching Appellants' "second mode." (*Id.*) The Examiner then relies on that

[18] The Final Office Action does not set forth the details of the claim rejections. Instead, it notes that the details of the rejections based are set forth in the previous office action

interpretation of Adolph, in asserting that cited aspects of only Adolph disclose Appellants' claimed "single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio." (*Id.*)

Appellants respectfully disagree, and submit that the Examiner is misinterpreting the teachings of Adolph. The Examiner is inconsistent in identifying the specific aspect of Adolph that allegedly teaches Appellants' claimed "first multiplexed stream." At one point the Examiner asserts that the output of "MMUX" of Adolph teaches Appellants' "first multiplexed stream," produced when operating in Appellants' claimed "first mode." (*See* 6/10/2010 Office Action at page 2.) However, at another point in the same rejection, the Examiner asserts, instead, that the output of "MUX 1" of Adolph teaches Appellants' "first multiplexed stream" produced by Appellants' claimed "multiplexing circuitry" when operating in Appellants' "second mode." (*Id.*) Thus, the Examiner alleges that two different elements of Adolph (that produce two different output signals, i.e., the output of "MUX 1" and the output of "MMUX"), both teach producing Appellants' "first multiplexed stream." Appellants respectfully submit that the "programme data stream" output by "MUX 1" of Adolph cannot teach Appellants' claimed "first multiplexed stream," because the "MUX 1" does not have as inputs the "first compressed video," "second compressed video," "first compressed audio," and "second compressed audio," required by claim 10 "when operating in the first mode." The Examiner appears to be

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mailed on 06/10/2010. (*See* Final Office Action at pp. 2-3, ¶¶ 2-9.)

changing the element identified as teaching the claimed "first multiplexed stream" in the cited art to suit his needs, without explanation. Such an inconsistent interpretation of the Adolph cannot provide the support required by M.P.E.P. §2142 for a *prima facie* case of obviousness. Accordingly, claim 10 is patentable because the proposed combination of Adolph and Hinchley fails to disclose or suggest multiplexer circuitry that operates in a first mode and a second mode in the manner required by claim 10.

The Examiner purports to respond to these arguments in the Final Office Action. (*See* Final Office Action at pp. 4-7.) In so doing, the Examiner states as follows:

> The examiner respectfully disagrees with the applicant. It is submitted that Adolph clearly teaches multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode), which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX I) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

(Final Office Action at p. 5.) Appellants disagree. Initially, as noted above, the Examiner takes inconsistent positions in attempting to construe Figure 3 as embodying the elements of claim 10. Moreover, in the above passage the Examiner merely recites the relevant language of claim 10 and cites to elements of Figure 3 of Adolph without identifying any text from Adolph to support his interpretation. Accordingly, by failing to

cite to any evidence to support this arbitrary and incorrect construction of Adolph, the Examiner has not established a *prima facie* case that claim 10 is unpatentable. *See In re Vaidyanathan*, Appeal 2009-1404 at pp. 18-19 (Fed. Cir. May 19, 2010) (nonprecedential) ("If the examiner is able to render a claim obvious simply by saying it is so, neither the Board nor [the Federal Circuit] is capable of reviewing that determination. . . . If there is **neither record evidence nor detailed examiner reasoning**, the Board should not conclude that ... claims are obvious."); *see also In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001) ("[T]he Board **cannot** simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, **the Board must point to some concrete evidence in the record in support of these findings**."); *see In re Wada and Murphy*, Appeal 2007-3733 (A proper rejection that an Examiner make "a searching comparison of the claimed invention – **including all its limitations** – with the teaching of the prior art."); *see also* MPEP §706.02(j) ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.")

Accordingly, claim 10 is patentable at least because the proposed combination of Adolph and Hinchley does not disclose or suggest a multiplexer circuitry that operates in a first mode and a second mode in the manner required by claim 10.

Claim 10 is also patentable because the proposed combination of Adolph and Hinchley does not disclose or suggest "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device" and "wherein

the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device." The Examiner alleges that Adolph satisfies these limitations as follows:

> Re claims 10 and 24, Adolph discloses a audio/video encoder device (fig. 3, a single device) comprising, on a single integrated circuit:
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> * * *
>
> wherein the device (fig. 3) transmits the first multiplexed stream (the output of MUX1, MUX1 of fig. 3)) to circuitry external (fig. 4) to the device (fig. 3) via a first output of the device (MOD and BBRF of fig. 3, transmitting the first output of the device (fig. 3)); and
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> wherein the device (fig. 3) transmits the second multiplexed stream (the output of MUX2, MUX2 of fig. 3) to circuitry external (fig. 4) to the device (fig. 3) via a second output of the device (MOD and BBRF of fig. 3, transmitting the second output (the output of MUX2) to the DMUX of fig. 4)

(*See* 6/10/2010 Office Action at pp. 2-3.) Hence, the Examiner has identified the "first multiplexed stream" and the "second multiplexed stream" as being produced by "MUX 1" and "MUX 2," respectively. (*Id.*) That is, Appellants' two streams are asserted to be taught by the two outputs of the "MUX 1" and "MUX 2" of FIG. 3, respectively. Appellants note, however, that the Examiner has not shown where Adolph teaches that the outputs of "MUX 1" and "MUX 2" of the transmitter of FIG. 3 of Adolph are transmitted to circuitry external to the device via a "first output of the device" and a "second output of the service," respectively. Instead, the Examiner identifies "MOD" and "BBRF" of FIG. 3 of Adolph as teaching both of Appellants' claimed "first output of the device" and "second output of the device." (*See* 6/10/22010 Office Action at page 3.) Adolph describes the "transport data stream" processed by the "encoder unit MOD"

and "modulator BBRF" as being "combined in a transport multiplexer MMUX." Therefore, Appellants respectfully submit that the "transport data stream" of Adolph is a single data stream output by the "transmitter" of FIG. 3. (*See* Adolph at 4:38-43.) The Examiner fails credibly to explain how the same "MOD" and "BBRF" elements that process a single data stream teach transmission of the two streams, namely Appellants' claimed "first multiplexed stream" and "second multiplexed stream", via the claimed "first output" and "second output," as required by claim 10. The Office does not provide the "explicit analysis" required by M.P.E.P. §2142 to explain how Adolph is being interpreted to teach what is asserted.

The Examiner responds to these arguments in the Final Office Action as follows:

> The applicant further argues that Adolph does not disclose transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and transmits the second multiplexed stream to circuitry external to the device via a second output of the device.
>
> The examiner strongly disagrees with the applicant. It is submitted that Adolph teaches the transport stream (output from MMUX of fig. 3, note MMUX of fig. 3 operates in the two modes, therefore the MMUX enables to multiplex the first multiplexed stream and the second multiplexed stream to produce the transport stream) comprises the first multiplexed stream, which comprises the first compressed video, first compressed video, second compressed video, and second compressed audio in the first mode or the first compressed video and first compressed audio in the second mode, and the second multiplexed stream, which comprises the second compressed video and second compressed audio, wherein the transport stream is transmitted by (SP, ERS, MOD, and BBRF of fig. 3) to circuit (e.g. fig. 4, REBB) external to the MMUX of fig. 3.

(*See* Final Office Action at p. 7.) Once again, the Examiner fails to cite to any evidence to support his interpretation of Adolph. Nothing in Adolph discusses or describes the two modes of operation that the Examiner alleges are present. Instead, Adolph describes operation of the transmitter as follows:

> FIG. 3 illustrates a block diagram of a transmitter for the transmission method according to the invention, two programmes being transmitted by way of example. Video and audio signals V1, A1, V2, A2 are each fed to a source coder VE1, AE1 and VE2, AE2, respectively. A common programme data stream is produced from the source-coded video and audio signals, together with supplementary data which are generated in a stage DE1 and DE2, respectively, in a programme multiplexer MUX1 and MUX2, respectively. The various (in the example of FIG. 3: two) programme data streams are then combined in a transport multiplexer MMUX to form a transport data stream in accordance with the MPEG2 system specification, the transport packets being identified on the basis of the packet identifiers.

(Adolph at 4:30-44.) As can be seen, nothing in this passage Adolph discloses or suggests two modes of operation. Nor has the Examiner cited to any text of Adolph to support his interpretation of this reference.

Therefore, claim 10 is patentable because the proposed combination of Adolph and Hinchley fails to disclose or suggest "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device" and "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device."

In addition, claim 10 requires "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder." The Examiner admits that Adolph

fails to disclose this limitation. (*See* 6/10/2010 Office action at page 3.) In an attempt to make up for this admitted deficiency, the Examiner turns to Hinchley. However, in proposing to combine Adolph and Hinchley, the Examiner fails to provide "articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness" in the detailed manner described in KSR.

Specifically, in order to support an assertion of obviousness, the Examiner is required to provide "some articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness." *See KSR International Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) quoting *In re Kahn*, 441 F.2d 997,988 (CA Fed. 2006). Put another way, the Examiner should "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR*, 127 S. Ct. at 1741. The Examiner should make "explicit" this rationale of "the apparent reason to combine the known elements in the fashion claimed," including a detailed explanation of "the effects of demands known to the design community or present in the marketplace" and "the background knowledge possessed by a person having ordinary skill in the art." *Id.*

In the present instance, the Examiner attempts to justify the combination of Adolph and Hinchley as follows:

> Taking the teachings of Adolph and Hinchley as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Hinchley into the system of Adolph to efficiently multiplex the incoming streams together and flexible to adjust the data rate for different formats.

(Final Office Action at p. 8.) This conclusory sentence is the entire extent of the Examiner's justification for alleging that it would be obvious to combine these references. This conclusory allegation does not provide "articulated reasoning with some rationale underpinning to support the legal conclusion of obviousness" in the detailed manner described in *KSR*. The Examiner apparently suggests that the addition of Hinchley would improve the efficiency and flexibility of Adolph. However, the Examiner provides absolutely no explanation of how the alleged efficiency and flexibility would be achieved. Hence, it is respectfully submitted that the Examiner has not established a *prima facie* case of obviousness and the Board should withdraw the rejection of claim 10.

In addition, the Examiner mischaracterizes the teaching of Hinchley. In rejecting claim 10, the Examiner alleges as follows:

> Hinchley teaches a single chip (120 of fig. 1) comprises the multiplexer (204 of fig. 2), encoders (208 of fig. 2), and control circuitry (250 of fig. 2) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (212, 214, 216, 218, and 220 of fig. 2).

(6/10/2010 Office Action at p. 3.) This portion of the rejection of claim 10 amounts to no more than a conclusory statement, in that the Office fails to provide the "explicit analysis" required by M.P.E.P. §2142 to explain why the cited art is interpreted in this way. The Examiner fails to cite any text from Hinchley to support the above statement. Appellants respectfully submit that such conclusory statements are insufficient to support a *prima facie* case of obviousness. *See* M.P.E.P. §2142; *see also See In re Vaidyanathan*, Appeal 2009-1404 at pp. 18-19 (Fed. Cir. May 19, 2010)

(nonprecedential) ("If the examiner is able to render a claim obvious simply by saying it is so, neither the Board nor [the Federal Circuit] is capable of reviewing that determination. . . . If there is **neither record evidence nor detailed examiner reasoning**, the Board should not conclude that ... claims are obvious."); *see also In re Zurko*, 258 F.3d at 1386 ("[T]he Board **cannot** simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, **the Board must point to some concrete evidence in the record in support of these findings**."); *see In re Wada and Murphy*, Appeal 2007-3733 (A proper rejection that an Examiner make "a searching comparison of the claimed invention – **including all its limitations** – with the teaching of the prior art."); *see also* MPEP §706.02(j) ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.").

A review of Hinchley shows that the entirety of Hinchley fails to make any mention of "synchronization." Cited element "250" of Hinchley, which has been identified by the Office as teaching Appellants' element "control circuitry," is identified by Hinchley as "multimedia processor 250." *See* Hinchley at 3:50. According to Hinchley, "[m]ultimedia processor 250 is preferably a Digital Signal Processing (DSP) core which is designed to perform conventional multimedia operations as well as the specialized functions in accordance with the present invention." *Id.* at 3:65-4:2. Nothing in Hinchley teaches or suggests that the "multimedia processor 250" "synchronizes" anything, let alone synchronizing the "multimedia encoder 208" and "stream processor 200" of Fig. 2, which have been identified by the Examiner as teaching Appellants' claim elements

"first/second encoder" and "multiplexer circuitry." Hinchley merely teaches that the "multimedia engine 250" adjusts a "data rate" of only an encoder, but says nothing about "synchronization." *Id.* at 6:13-8:44. Indeed, Hinchley fails to make any mention of "synchronization" of anything in its entirety, let alone of the elements and the manner claimed. Adjusting a "data rate" is quite different from "synchronization," as claimed.

Accordingly, clam 10 is also patentable because the proposed combination of Adolph and Hinchley fails to disclose or suggest "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder," as required by claim 10.

Therefore, based at least upon the above, Appellants respectfully submit that the Examiner has not shown that the cited art teaches all aspects of Appellants' claim 10, that the Examiner has not established a *prima facie* case of obviousness, and that claim 10 is allowable over the cited art.

Independent claims 24 is similar in relevant respects to claim 1. Therefore, claim 24 is patentable over the proposed combination of Adolph and Hinchley for at least the reasons stated above regarding claim 1.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 10 and 24.

B. Claims 11-23 And 25-33

Claims 11-23 and 25-33 depend on independent claims 10 and 24, respectively. Therefore, claims 11-23 and 25-33 are patentable over the proposed combination of

Adolph and Hinchley for at least the reasons stated above with regard to claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 11-23 and 25-33.

II. CLAIMS 21, 22, 34, AND 35 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF ADOLPH, HINCHLEY, AND ISHIHARA DOES NOT RENDER

Claims 21 and 22, and claims 34 and 35 depend, respectively, from independent claims 10 and 24. Therefore, these claims are allowable over the proposed combination of Adolph and Hinchley for at least the reasons stated above with regard to claims 10 and 24. Ishihara fails to overcome the deficiencies noted above with regard to Adolph and Hinchley. Accordingly, claims 21, 22, 34 and 35 are patentable over the proposed combination of Adolph, Hinchley and Ishihara for at least the reasons stated above in connection with claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 21, 22, 34 and 35.

III. CLAIMS 23 AND 36 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF ADOLPH, HINCHLEY, ISHIHARA, AND KOPET

Claims 23 and 36 ultimately depend from independent claims 10 and 24, respectively. Therefore, these claims are allowable over the proposed combination of Adolph and Hinchley for at least the reasons stated above with regard to claims 10 and 24. Ishihara and Kopet fail to overcome the deficiencies noted above with regard to Adolph and Hinchley. Accordingly, claims 23 and 36 are patentable over the proposed

combination of Adolph, Hinchley, Ishihara and Kopet for at least the reasons stated above in connection with claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 23 and 36.

IV. CLAIMS 10-12, 15-16, 20, 24-25, 28-29, AND 33 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY AND ADOLPH

A. Independent Claims 10 And 24

Claim 10 is patentable because the proposed combination of Krishnamurthy and Adolph fails to disclose or suggest at least the following element of claim 10:

> A single-chip audio/video encoder device comprising, on a single integrated circuit: multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio....

As can be seen above, Appellants' claimed "first mode" and "second mode" characterize operation of Appellants' claimed "multiplexer circuitry," in which in the claimed "first mode," the "multiplexer circuitry" produces a "first multiplexed stream" using four components, namely, "first compressed video," "first compressed audio," "second compressed video," and second compressed audio." In the claimed "second mode," however, the "multiplexer circuitry" produces the "first video stream" using the two components "first compressed video" and "second compressed video," and

produces, in addition, a "second multiplexed stream" using the two components "second compressed video" and "second compressed audio." Thus, the "first mode" and "second mode" define the video and audio content of the "first multiplexed stream" and the "second multiplexed stream."

In rejecting claim 10, the Examiner alleges as follows:

> Re claims 10 and 24, Krishnamurthy teaches . . . multiplexer circuitry (308 of fig. 3) that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode), which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3);

(6/10/2010 Office Action at page 8.) Thus, the Examiner asserts that col. 20, lines 22-25 of Krishnamurthy alone teach Appellants' claimed "first mode" and "second mode." Appellants respectfully disagree. In context, the passage cited by the Examiner reads as follows:

> Each SSI serial input port 336 has three wires carrying a clock signal (sclk), a data signal (sdat), and a frame signal. All 24 clock signals sclk should be configured as the input clock signals and connected to an on-board 27-MHz clock oscillator 504. 27-MHz clock 504 will also be used as the DSP clock, and on-chip PLL circuits will generate a 90-MHz DSP clock. In that case, on-chip timers can be used for the PCR time-base corrections. The frame signals will indicate whether or not the data signal sdat carries meaningful data. The data signals sdat are burst with a maximum rate of 27 Mbps. The frame signals can also be programmed in a "multi-channel mode" to send multiple packets into assigned

> on-chip buffers for transmitting the individual encoders' statistical parameters.

Krishnamurthy at 20:12-25 (Where lines 22-25 are indicated with underlining.) The above passage of Krishnamurthy teaches that "frame signals will indicate whether or not the data signal sdat carries meaningful data" and can be programmed in "multi-channel mode," to "send multiple packets into assigned on chip buffers for transmitting the individual encoders' statistical parameters." Thus, Krishnamurthy clearly teaches that the disclosed "multi-channel mode" relates not to operating modes that define video and audio content of multiplexed streams, but instead to transmission of **statistical parameters** of encoders.

Accordingly, Appellants submit that claim 10 is patentable because the proposed combination of Krishnamurthy and Adolph fails to disclose or suggest multiplexer circuitry that operates in a "first mode" **and** "second mode" in the manner required by claim 10.

Claim 10 is also patentable because the proposed combination of Krishnamurthy and Adolph fails to disclose or suggest "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device," **and** "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," as required by claim 1. The Examiner alleges that Krishnamurthy satisfies this aspect of claim 10 as follows:

> Re claims 10 and 24, Krishnamurthy teaches . . . wherein the device (fig. 3, see also fig. 5) transmits the first multiplexed stream to circuitry external (506 of fig. 5, col. 20, lines 27-28) to the device via a first output of the device; and wherein the device (fig. 5) transmits the second multiplexed

> stream to circuitry external (506 of fig. 5; col. 20, lines 27-28) to the device via a second output of the device.

(6/10/2010 Office Action at pages 8-9.) Accordingly, the Examiner asserts that FIG. 3 and FIG. 5 of Krishnamurthy teach Appellants' claimed "single-chip audio/video encoder device." (*Id.* at p. 8, lines 1-3.) Krishnamurthy describes FIG. 3 as a "system-level block diagram of computer system, according to one embodiment of the present invention," and FIG. 5 as "a board-level block diagram of the statistical multiplexing board of the computer system of FIG. 3." *See id.* at col. 4, lines 9-15. The Examiner identifies a single element 506 of FIG. 5 (which Krishnamurthy teaches corresponds to element 308 of FIG. 3) as teaching **both** of Appellants' claim features (1) "wherein the device transmits the first multiplexed stream to circuitry external to the device **via a first output of the device**," and (2) "wherein the device transmits the second multiplexed stream to circuitry external to the device **via a second output of the device**."

Claim 10 recites first and second outputs of the device. FIG. 5 of Krishnamurthy, however, does not disclose element 506 as having two outputs. In the rejection, the Examiner cites the following passage of Krishnamurthy:

> ASI interface 506 uses a TAXI transmitter chip with parallel interface from Advanced Micro Devices, such that there are FIFO and CPLD control circuits to handle the TAXI interface and ASI controls.

(Krishnamurthy at 20:27-38.) Nothing in this passage discloses or suggest transmitting two streams of multiplexed video/audio. In fact, this passage describes element 506 as an ASI interface, where ASI stands for Asynchronous Serial Interface. Notably, in rejecting the claim, the Examiner points twice to the same element (506 of Figure 5) and

text (col. 20, lines 27-28) as allegedly disclosing the two outputs recited in claim 10. The Examiner fails to demonstrate where Krishnamurthy discloses or suggests two of element 506 acting as outputs of the "stat mux board" of FIG. 5. Nor does the Examiner show that Krishnamurthy discloses or suggests that the "computer system" of FIG. 3 includes more that one "stat-mux board 308." The presence of a single element 506 [308] in the "stat mux board" of Krishnamurthy is consistent with the clear statement by Krishnamurthy that its disclosure "relates to the compression and transmission of video signals, and, in particular, to the compression and transmission of multiple compressed video streams over a **single**, shared communication channel." (Krishnamurthy at 1:15-19.) Therefore, Appellants respectfully submit that the disclosure of Krishnamurthy consistently does not disclose or suggest a "second multiplexed stream" transmitted via a "second output," and therefore does not teach, suggest, or disclose at least Appellants' claim feature "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," as claimed. The Examiner seemingly recognizes this at page 9 of the Office action, which states, in part:

> Krishnamurthy does not particularly teach when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio as claimed.

(6/10/2010 Office Action at page 9.) The Examiner, however, then mistakenly relies upon Adolph, stating the following:

> Adolph teaches which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed

> stream (the output of MUX I) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

(6/10/2010 Office Action at p. 9.) Here, the Office asserts that Adolph teaches producing Appellants' claimed "first multiplexed stream" and "second multiplexed stream." Appellants respectfully submit, however, that Adolph does not disclose or suggest that the "transmitter" of FIG. 3 of Adolph transmits the output of "MUX 1" to circuitry external to the "transmitter" via a first output of the "transmitter" **and** transmits the output of "MUX2" to circuitry external to the "transmitter" via a second output of the "transmitter," in accordance with Appellants' claim 10. It is quite clear from even a cursory review of FIG. 3 of Adolph that the outputs of "MUX 1" and "MUX 2" of the "transmitter" pass to element "MMUX" that produces a single output passed to element "SP", which eventually exits from the "transmitter" as a single output "BBRF."

Accordingly, claim 10 is patentable because the proposed combination of Krishnamurthy and Adolph fails to disclose or suggest "wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device," **and** "wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device," as required by claim 10.

Claim 10 is also patentable because the cited combination of Krishnamurthy and Adolph fail to disclose or suggest "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder. . . ," as recited in claim 10. The Examiner alleges as follows regarding this element of claim 10:

> Re claims 10 and 24, Krishnamurthy teaches . . . control circuitry (304 of fig. 3, note the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all element as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder."

(6/10/2010 Office Action at page 8.) Appellants disagree with the Examiner's analysis. The Examiner cites to Figure 3 of Krishnamurthy, which is reproduced below for reference:

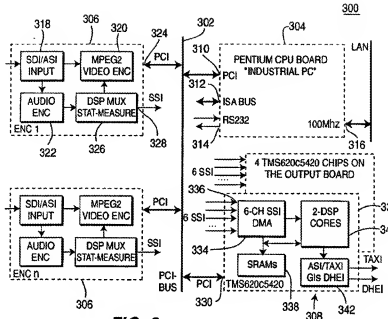

FIG. 3

Krishnamurthy describes Fig. 3 as follows:

> FIG. 3 shows a system-level block diagram of computer system 300, according to one embodiment of the present invention. Computer system 300 is a PCI bus-based industrial PC (Personal Computer) enclosure with multiple PCI boards. In particular, computer system 300 comprises a PCI bus 302 configured with a Central Processing Unit (CPU) board 304, up to n=24 encoder boards 306, and a statistical multiplexing (stat-mux) board 308. Although computer system 300 relies on a PCI bus, it will be understood that any other suitable system bus could be used in alternative embodiments of the present invention.

Id. at 18:9-19. There simply is no reference in this passage (or elsewhere in Krishnamurthy) that says anything about "synchronization" by "CPU board 304", or any other element of Fig. 3. of Krishnamurthy, of the other elements of the "computer system" of Fig. 3, which the Office has identified as teaching Appellants' "single-chip audio/video encoder device."

In making the rejection, the Examiner alleges "the CPU would obviously synchronize all elements as described in figure 3 . . . ." (*See* 6/10/2010 Office Action at 8.) The Examiner provides absolutely no support for this conclusion. In the absence of any support, Appellants are left to conclude that the Office is impliedly asserting that synchronization of the "encoder board 306" and "stat-mux board 308", which the Office identified as teaching Appellants' features "first encoder", "second encoder", and "multiplexer circuitry", by the "CPU board 304", is inherent.

According to MPEP §2112, Sec. IV, page 2100-54,55, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, **may not be established by probabilities or possibilities**. The mere fact that a certain thing **may** result from a given set of circumstances **is not sufficient**.'" In addition, M.P.E.P. §2112 recognizes that the courts have made clear that "In relying upon the theory of inherency, the examiner **must** provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic **necessarily** flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990)." (Emphasis in original).

Appellants respectfully maintain that the Examiner has failed to meet the requirements for an assertion of inherency, by failing to provide a basis in fact and/or technical reasoning to reasonably support the determination that "the CPU would obviously synchronize all elements as described in figure 3" **necessarily** flows from the

teachings of the applied prior art. Therefore, Appellants respectfully submit that the Examiner has failed to show that (CPU board 304) would inherently synchronize the "encoder board(s) 306" and "stat-mux board 308" of the "computer system 300" of Krishnamurthy.

Indeed, Krishnamurthy clearly states as follows

> **Since the applications are not synchronized at the frame level, a frame-level target is computed for the encoder that will start encoding a frame next (at any given time)**, based on the average MQUANT chosen for that encoder. Using a rate-distortion model linking bit consumption, average MQUANT, and motion compensated distortion, and enforcing constraints on MQUANT, the bit count for a frame can be estimated from prior data. An example of the constraint on MQUANT can be that the quality is uniform across the applications, while ensuring that the temporal rate of change of average MQUANT is within a tolerance threshold. The channel bit rate is divided between the applications according to their respective complexities and relative significance. The complexities are updated on the fly, and the relative significance can be obtained from the results of off-line profiling stored in application profiles server 124.
>
> For the less controllable encoders, only the frame-level target (or average MQUANT) might be able to be communicated to the encoder. For the more controllable encoders, the basic unit of operation will be a slice (e.g., a row of macroblocks). **Because the encoders are not synchronized**, this will require a worst-case buffer requirement of 2 slices. A slice-level target is computed for each controllable encoder based on the frame target, the buffer fullness for that encoder (which is indicative of the buffer delay), and the instantaneous bit rate available after deducting the bits (within a latency window) from the less controllable encoders. The slice targets are also constrained by the fact that MQUANTs cannot change too much within a frame.

(Krishnamurthy at 10:60 to 11:20.) The above passages clearly contradict the Examiner's allegation that "the CPU would obviously synchronize all elements as described in figure 3."

If the Examiner did not mean to assert inherency, then Appellants respectfully submit that the Examiner has failed to provide any basis or support for concluding that this aspect of Appellants' claim 10 is obvious. In this regard, Appellants note "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." M.P.E.P. §2142. In this instance, the Examiner fails to provide such an "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness", required by the courts. Further, M.P.E.P. §2142 states that "[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious." However, no such "articulation of the reason(s) why the claimed invention would have been obvious" has been provided by the Office to support the rejection of this aspect of Appellants' claim 10.

In responding to Appellant's arguments regarding this element of claim 10, the Examiner states as follows:

> The applicant further argues that Krishnamurthy does not teach, suggest, or render obvious controller circuitry that synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.
>
> The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable

to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, harmonize, or orchestrate operation of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuit properly working.

Krishnamurthy further discloses Computer systems in accordance with the present invention avoid PCI bus delay by using the built-in multi-channel Synchronized Serial Interface (SSI) ports of multiple Digital Signal Processors (DSPs), where each DSP performs video and audio encoder control, PES/TS layer multiplexing, and computation of statistical measurements of its corresponding video stream payload. The DSPs' on-chip memories may also eliminate the need for bitstream First-In, First-Out (FIFO) chips and some common SDRAM (Synchronized Dynamic Random Access Memory) chips (col. 17, line 65-col. 18, line 8). There is CPLD (Complex Programmable Logic Device) or FPGA (Field-Programmable Gate Array) based deframing firmware to split the video and audio data, and to reproduce the video synchronization signals for the MPEG2 video encoder chip (col. 19, lines 18-22), the above disclosure is evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit.

Krishnamurthy further teaches a Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3, so the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuits properly working. Since Krishnamurthy teaches the MPEG-2 encoder chip that would obviously has a control function to synchronize the multiplexer, audio and video encoders according the MPEG-2 standards, therefore one of ordinary skill in the art to modify the control function according to MPEG-2 into the CPU (304 of fig. 3) to perform synchronization. In view of the discussion above, the claimed features are unpatentable over Krishnamurthy.

(Final Office Action at 22-23.) Appellants respectfully submit that Krishnamurthy's teaching of a "Central Processing Unit (CPU) (304 of fig. 3) that is programmable to control all elements in the circuit board of figure 3" is insufficient to establish a *prima facie* case that "the Central Processing Unit (CPU) (304 of fig. 3) would synchronize, coordinate, or harmonize all operations of the first encoder circuitry (306 of fig. 3), the second encoder circuitry (306n of fig. 3), and the multiplexer circuitry (308 of fig. 3) in order for all circuits properly working." Nor, is Krishnamurthy's teaching of "avoiding PCI bus delay," in the manner described in the Final Office Action, "evidence that the Krishnamurthy's controller circuitry synchronizes operation of the first encoder, the second encoder and the multiplexer circuit." Indeed, as Appellants have previously shown Krishnamurthy teaches "[s]ince the applications are not synchronized at the frame level, a frame-level target is computed for the encoder that will start encoding a frame next (at any given time)." Krishnamurthy at 10:60-62. Similarly, Krishnamurthy also clearly states "the encoders are not synchronized." *Id.* at 11:13.

Hence, the Examiner's statement that "the CPU would obviously synchronize all elements as described in figure 3" simply is not true. The Examiner attempts to support this contention by merely citing to Figure 3. The Examiner has not identified any credible support in the text of Krishnamurthy for his conclusory statement that "the CPU would obviously synchronize all elements as described in figure 3." As a matter of law, such unsupported, conclusory statements are insufficient to support a *prima facie* case of obviousness. *See* M.P.E.P. §2142; *see also See In re Vaidyanathan*, Appeal 2009-1404 at pp. 18-19 (Fed. Cir. May 19, 2010) (nonprecedential) ("If the examiner is able to render a claim obvious simply by saying it is so, neither the Board nor [the Federal

Circuit] is capable of reviewing that determination. . . . If there is **neither record evidence nor detailed examiner reasoning**, the Board should not conclude that ... claims are obvious."); *see also In re Zurko*, 258 F.3d at 1386 ("[T]he Board **cannot** simply reach conclusions based on its own understanding or experience – or on its assessment of what would be basic knowledge or common sense. Rather, **the Board must point to some concrete evidence in the record in support of these findings**."); *see In re Wada and Murphy*, Appeal 2007-3733 (A proper rejection that an Examiner make "a searching comparison of the claimed invention – **including all its limitations** – with the teaching of the prior art."); *see also* MPEP §706.02(j) ("It is important for an examiner to properly communicate the basis for a rejection so that the issues can be identified early and the applicant can be given fair opportunity to reply.").

By citing only an isolated element in a figure of Krishnamurthy, without supporting text or any interpretation, and without the "explicit analysis" required by M.P.E.P. §2142, has not established a *prima facie* case of obviousness with respect to Appellants' feature "control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder." Accordingly, Appellants submit that the proposed combination of Krishnamurthy and Adolph does not teach, suggest, or disclose at least this aspect of claim 10, that the Office has therefore not shown that the cited art teaches all aspects of claim 10, and that a *prima facie* case of obviousness has not been established. Accordingly, Appellants respectfully submit that claim 10 is not rendered unpatentable, and that claim 10 and any claims that depend therefrom are allowable over the cited art for at least this additional reason.

For at least the reasons set forth above, claim 10 is patentable over the proposed combination of Krishnamurthy and Adolph. Independent claims 24 is similar in relevant respects to claim 1. Therefore, claim 24 is patentable over the proposed combination of Kirshnamurthy and Adolph for at least the reasons stated above regarding claim 1.

Appellant reserves the right to argue additional reasons beyond those set forth above to support the allowance of claims 10 and 24.

B. Claims 10-12, 15-16, 20, 24-25, 28-29 and 33

Claims 10-12, 15-16, 20, 24-25, 28-29 and 33 each ultimately depend on one of independent claims 10 and 24. Therefore, 10-12, 15-16, 20, 24-25, 28-29 and 33 are patentable over the proposed combination of Kirshnamurthy and Adolph for at least the reasons stated above with regard to claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 10-12, 15-16, 20, 24-25, 28-29 and 33.

V. CLAIMS 13 AND 26 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY, ADOLPH, AND BRUCK

Claims 13 and 26 depend from independent claims 10 and 24, respectively. Therefore, these claims are allowable over the proposed combination of Kirshnamurthy and Adolph for at least the reasons stated above with regard to claims 10 and 24. Bruck fails to overcome the deficiencies noted above with regard to Kirshnamurthy and Adolph. Accordingly, claims 13 and 26 are patentable over the proposed combination of Kirshnamurthy, Adolph and Bruck for at least the reasons stated above in connection with claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 13 and 26.

VI. CLAIMS 14, 17-19, 27 AND 30-32 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY, ADOLPH, AND HINCHLEY

Claims 14 and 17-19, and claims 27 and 30-32 depend, respectively, from independent claims 10 and 24. Therefore, these claims are allowable over the proposed combination of Kirshnamurthy and Adolph for at least the reasons stated above with regard to claims 10 and 24. Hinchley fails to overcome the deficiencies noted above with regard to Kirshnamurthy and Adolph. Accordingly, claims 14, 17-19, 27 and 30-32 are patentable over the proposed combination of Kirshnamurthy, Adolph and Hinchley for at least the reasons stated above in connection with claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 14, 17-19, 27, and 30-32.

VII. CLAIMS 21, 22, 34, AND 35 ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY, ADOLPH, AND BOICE

Appellants respectfully submit that claims 21-22 and 34-35 depend from independent claims 10 and 24, respectively. Therefore, these claims are allowable over the proposed combination of Kirshnamurthy and Adolph for at least the reasons stated above with regard to claims 10 and 24. Boice fails to overcome the deficiencies noted above with regard to Kirshnamurthy and Adolph. Accordingly, claims 21-22 and 34-35 are patentable over the proposed combination of Kirshnamurthy, Adolph and Boice for at least the reasons stated above in connection with claims 10 and 24.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 21-22 and 34-35.

VIII. CLAIMS 21-22 (OR 23) AND 34-35 (OR 35) ARE PATENTABLE OVER THE PROPOSED COMBINATION OF KRISHNAMURTHY, ADOLPH, BOICE, AND KOPET

As an initial matter, Item 9 of the Final Office Action (*see id.* at page 3) rejects claims 21-22 and 34-35 over Krishnamurthy, Adolph, Boice, and Kopet. Appellants respectfully note, however, that claims 21-22 and 34-35 were rejected in Item 8 of the Final Office Action (*see id.* at page 3) over Krishnamurthy, Adolph and Boice. The detailed discussion of the rejection, however, appears to be directed to the limitations recited in claims 23 and 35.

In any event, claims 21-22 (and 23) and 34-35 (and 36) depends from independent claims 10 and 24, respectively. Appellants respectfully submit that claims 10 and 24 are allowable over the proposed combination of references, in that the Office has not shown how and why Kopet remedies the deficiencies of Krishnamurthy, Adolph, and Boice, set forth above. Because independent claims 10 and 24 are allowable over the proposed combination of references, Appellants respectfully submit that claims 21-22 (or 23) and 34-35 that depend therefrom are also allowable, for at least the same reasons.

Appellants reserve the right to argue additional reasons beyond those set forth above to support the allowance of claims 21-22 (and 23) and 34-35 (and 36).

CONCLUSION

Appellants respectfully submit that the pending claims of the present application should be in condition for allowance for at least the reasons discussed above, and request reconsideration of the claim rejections. The Commissioner is authorized to charge the fee for this Appeal Brief ($540), and any additional fees or credit overpayment to Deposit Account 13-0017.

Respectfully submitted,

Date: May 16, 2011

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CLAIMS APPENDIX
(37 C.F.R. § 41.37(c)(1)(viii))

10. A single-chip audio/video encoder device comprising, on a single integrated circuit:

multiplexer circuitry that operates in a first mode and a second mode, which when operating in the first mode produces a first multiplexed stream from first compressed video, first compressed audio, second compressed video, and second compressed audio; and which when operating in the second mode concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio;

a first encoder that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

11. The device according to claim 10, wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder.

12. The device according to claim 10, wherein the first encoder and the second encoder operate concurrently.

13. The device according to claim 10, wherein the first encoder and the second encoder perform luminance and chrominance filtering.

14. The device according to claim 10, wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data.

15. The device according to claim 10, wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals.

16. The device according to claim 15, wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface.

17. The device according to claim 15, wherein the at least one bus interface is configurable to act as a bus master using direct memory access.

18. The device according to claim 15, wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

19. The device according to claim 15, wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface.

20. The device according to claim 10, wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels.

21. The device according to claim 10, wherein the first encoder and the second encoder each comprise a plurality of search processors for performing motion analysis.

22. The device according to claim 21, wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock.

23. The device according to claim 21, wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions.

24. A single-chip audio/video encoder device comprising, on a single integrated circuit:

control circuitry that synchronizes a first encoder, a second encoder, and multiplexing circuitry to produce a first multiplexed stream from first uncompressed video data, first uncompressed audio data, second uncompressed video data, and

second uncompressed audio data, when the multiplexing circuitry operates in a first mode, and to concurrently produce the first multiplexed stream from the first uncompressed video data and the first uncompressed audio data and a second multiplexed stream from the second uncompressed video data and the second uncompressed audio data, when the multiplexing circuitry operates in a second operating mode;

a first input for receiving the first uncompressed video data and first uncompressed audio data from a first source external to the device;

a second input for receiving second uncompressed video data and second uncompressed audio data from a second source external to the device;

wherein the device transmits the first multiplexed stream to circuitry external to the device via a first output of the device; and

wherein the device transmits the second multiplexed stream to circuitry external to the device via a second output of the device.

25. The device according to claim 24, wherein the encoding of the first multiplexed stream and the encoding of the second multiplexed stream is performed concurrently.

26. The device according to claim 24, wherein encoding of one or both of the first uncompressed video data and/or the second uncompressed video data comprises luminance and chrominance filtering.

27. The device according to claim 24, wherein the device comprises at least one interface for direct connection to external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data.

28. The device according to claim 24, wherein the device comprises at least one bus interface that is configurable to operate to couple the control circuitry and at least one controller external to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals.

29. The device according to claim 28, wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface.

30. The device according to claim 28, wherein the at least one bus interface is configurable to act as a bus master using direct memory access.

31. The device according to claim 28, wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

32. The device according to claim 28, wherein encoding and/or multiplexing is performed by microcode instructions received by the device via the at least one bus interface.

33. The device according to claim 24, wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels.

34. The device according to claim 24, wherein the encoding of one or both of the first uncompressed video data and/or the second uncompressed video data is performed by a plurality of search processors for performing motion analysis.

35. The device according to claim 34, wherein the plurality of search processors operate in parallel, each upon a different portion of a macroblock.

36. The device according to claim 34, wherein the plurality of search processors operate in parallel upon a single macroblock, each search processor operating at a different one of a plurality of resolutions.

EVIDENCE APPENDIX
(37 C.F.R. § 41.37(c)(1)(ix))

- U.S. Patent 5,825,430 ("Adolph") entered into the record in the Office Action mailed June 10, 2010.
- U.S. Patent 6,490,250 ("Hinchley") entered into the record in the Office Action mailed April 10, 2008.
- U.S. Patent 6,516,031 ("Ishihara") entered into the record in the Office Action mailed October 16, 2008.
- U.S. Patent 6,823,013 ("Boice") entered into the record in the Office Action mailed April 10, 2008.
- U.S. Patent 6,519,289 ("Bruck") entered into the record in the Office Action mailed November 16, 2010.
- U.S. Patent No. 6,665,872 ("Krishnamurthy") entered into the record in the Office Action mailed April 10, 2008.
- U.S. Patent No. 5,448,310 ("Kopet") entered into the record in the Office Action mailed October 16, 2008.

RELATED PROCEEDINGS APPENDIX
(37 C.F.R. § 41.37(c)(1)(x))

Appellants are unaware of any related appeals or interferences.